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Design of 32 Bit Low Power and High Speed Square Root Carry Select Adder

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Abstract

In this paper, the specifications to be considered while designing any integrated circuits including adder circuit are power, speed and area. Now a days even a small device require a basic needs, which should be highly efficient and low power, so here we came up with the flip flop. Without the use of adders and multipliers, the arithmetic operation in the digital system became incomplete. As we know that the Carry Select Adder (CSLA) is one of the fastest adder which performs the Arithmetic functions rapidly, it is clear that there is scope for reducing the area and power consumption in CSLA and one of the special case of CSLA is Square root carry select adder (SCSLA). Since SCSLA operates at high speed and reduce the power dissipation. In order to reduce both the power and area, the proposed technique of Adaptive voltage level at source (AVLS) with True Single Phase Clocking (TSPC) based D flip flop is used instead of using Ripple Carry Adder (RCA) and Binary to Excess converter(BEC). This can make less number of transistor counts with significant power and area. In this paper, a 32 bit square root carry select adder is implemented using AVLS-TSPC based D flip-flop.

Keywords: Carry select adder (CSLA), Square root carry select adder (SCSLA), D Flip-flop, Low power, High speed, True single phase clocking(TSPC).

1. Intoduction

Arithmetic circuits such as addition, subtraction, multiplication, address calculation, media access control address (MAC) unit, etc. are used to perform various computing purpose. Low-power calculation circuits play a vital role in the VLSI industry. For processor such as, the adders are the requisite building blocks of the digital signal processor. The MAC unit consumes a full adder, which crucially alter the efficiency of the overall system. Multiplication is too a mandatory arithmetic operation implemented by adding partial products .Therefore, a low power adder becomes necessary for achieving high performance processors and systems. Due to the propagation of the carry signal, the addition in the adders gets bounded. Carry select adder (CSLA) is superior to ripple carry adder (RCA) as it has a lesser amount of delay. In view of the carry propagation design for adders, an sustainable understanding can be achieved between cost and performance while using the carry select method. Linear CSLA uses two rows of RCAs, one in force with carry_ in = “0” and the other with carry_ in = “1” and as a result, two fixed sets of sum and carry_ out signals are acquired.

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The specific output is specified using the original carry_ in. The square root carry select adder (SCLSA) is a deviation of CSLA. The SCSLA design is a creation over the standard (linear) CSLA in terms of power dissipated and in force speed [5]. Carry is generated to succeeding blocks through multiplexers. Due to the addition of additional RCAs in SCSLA, it takes extra power as compared to RCA. Hence, it becomes essential to lower the power utilization of SCSLA to implement it in low-power applications. Using true single-phase clock (TSPC)-based D flip-flops in place of RCAs, the SCSLA can be made with reduced power. The TSPC-based D flip-flop is a dynamic CMOS-based flip-flop that focuses in working at a high speed. However, in an attempt to further reduce the utilization of power by SCSLA, the adaptive voltage level at source (AVLS) loom has been included. Adaptive voltage level at source is a technique in which the power utilization is condensed by decreasing the supply potential. A sleep-control signal, generally a clock signal, is used to standardize the operation of the AVLS circuit's transistors. It decreases the voltage across the gate source and drain, hence, reduce the outflow power. The AVLS circuit's output act towards as the supply voltage for the SCSLA.

This study point up on proposing a 32-bit SCSLA architecture that drains low power with a reduced amount of carry rippling delay. The proposed SCSLA uses AVLS logic with TSPC-based D flip flops as an alternative of RCAs. By combining AVLS and TSPC-based methodology in the proposed adder, the power and speed specifications are improved respectively. Modulation genius is bringing into effective action to understand the proposed structural design, while the recreation is carried out on modulation Spectre. The paper is classified into a variety of sections. Structures, Methodology, and realizations are discussed in section II. Section III demonstrates the CSLA and the AVLS methodology. The execution of the TSPC-based circuits and proposed structural design is explained in section IV. Section V examines the recreation results and compete with the proposed adders to the existing adder, regarding the use of power and lag specifications. Section VI finalize the work and suggest the future scope to it.

2. Literature Survey

The arithmetic, as well as logic units in microprocessors and microcontrollers, includes full adder which behave as the fundamental arithmetic circuit. Hence, in general the ability of circuits that includes the full adder can be customized by recovering the performance of the adder. Yamini devi, Rao and Locharla [2] described the reduction in area, in which the CSLA with add one circuit is used. Here the performance in terms of area and delay is connected using Leonardo spectrums, which are estimated for Square root CSLA using adds one circuit. The construction of the CSLA was altered to beat the power drain problems [5]. A TSPC-based D-FF was used to restore the carry input block. The recommended construction was enhanced with regard to power as well as area when come up to the standard and CSLA based on binary to excess-1 converter (BEC). Priyanka Sharma and Rajesh Mehra[6] suggested a new approach for low-power application, by using D flip-flops with reduced power utilization.

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The understanding of latches and flip-flops was accomplished by this tactics of the TSPC circuit which pointed the bias supply in the clock. By simulating AVLS into the circuits based on TSPC, the intention of low-power was also attained. Adaptive voltage level at source was observed to make use of decrease in power when modified with that of adaptive voltage level at ground (AVLG). Therefore, it was then included with TSPC-based flip-flop. The TSPC circuit was intended using 10T. There is a necessitate for a quicker arithmetic processing unit due to quick development in the technology worn these days, therefore, CSLA was well thought-out. Linear CSLA was bringing about in Sharanabasappa and Ravibabu [4] by replacing RCA with BEC. The authors also execute a new outlook of using D-latch so as to additionally minimize the power exploitation. The conclusion illustrates the diminution of delay of CSLA structural design than the existing models of BEC based CSLA design and RCA-based frameworks.

With capable procedure of area and minimizing the power drain of the adder, the complete presentation of the processors can be improved. In the authors optional the opinion of applying TSPC-based D-FF in place of using RCA and BEC in the conservative method. This model of 32-bit CSLA with normal TSPC-based D-FF used a smaller amount transistors counts as bear comparison with RCA. Therefore, the power utilize was not as much of compared to other circuits. The performance of D-FF that triggers at the positive edge of the clock along with customized TSPC end in reduced power utilization and the product of power-delay was compact [3] .

Ponnusamy and Palaniappan [9] perform a negative edge-triggered D-FF instead of the regular D-FF with the 32-bit CSLA. This constant shift of inputs directly affect the outputs of the adder on the purpose of the allow signal. Their method was put in practice in a portion out of Dadda multiplier by means of the micro wind tool that functions at a rapid pace. Conclusions were noticeable with the length and width exchange for power.

A new design known as TSPC flip-flop was used to pay off for the invention of drainage current at active nodes of the transistor. B.S.Premananda et. al., [1] put forward this approach for reduction in power and for surrounding an enormous range of operational frequencies in the CMOS processes. A gated inverter (GI) was worn to make three feedback circuits which were then used to execute the proposed method of TSPC-based flip-flop. The proposed design was produced with a 1 V power supply and is functioned at 2 GHz frequency. The results come to an end, that the suggested TSPC-based flip-flop shows zero error at low frequencies of 1 MHz.

The consideration of numerous models of D flip-flop pivot on the TSPC rationale which allow to tackle the plan of D-FF with a more reserved region and lower power usage when modified with the master–slave arrangement-based D flip-flop [7]. The paper weighs up the implementation of different TSPC-based D flip-flops and their connection concerning power, delay, and transistors. In converse with other flip-flops, it was seen that the 5T TSPC-

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based D-FF is superior in completing with less consumption of power from the evaluation result and analysis.

The upgrade of power plays a vital role in low-voltage and low-power applications. [11] Introduce a structural design of a D-FF circuit, which uses AVL methods for reduced power activity. The understanding of this D-FF was done by manipulate of H-Spice with 130 nm technology. Results of recreation make known of a limited power for the recommended cell, which modifies the AVL procedure. Removals of pointless switching of the transistors, with respect to the clock signal in memory elements, establish that the power drain can be bringing down to an outsized coverage than the current method. The AVLS technique had a power utilization of 1.13 nW, whereas the AVLG technique had a power depletion of 2.25 nW. Carry select adder proposed in [8] run through a marginal power but holds further area as adiabatic logic is included in the propose of the adder. There is a necessitate to design a SCLSA which lower the power, delay, and area.

3. Exiting System

The existing system of 32- bit adder, in which the addition using 32 –bit RCA get slower due to cascade of one bit full adder. In order to reduce the delay of RCA , 32-bit SCSLA with RCA is designed. Here the power consumption of the 32-bit SCSLA with RCA is greater than the power consumption of 32-bit RCA. For efficient usage of area and reduction in power dissipation of the adder we can go with proposed method.

4. Proposed System

The proposed method is that the 32-bit adder with SCSLA can be made low power using true single-phase clock (TSPC)-based D flip-flops in the place of RCAs. The TSPC-based D flip-flop is a dynamic CMOS-based flip-flop that aims at Low Power Square Root Carry Select Adder operating at a high speed. However, in an effort to further lower the consumption of power by SCSLA, the adaptive voltage level at source (AVLS) approach has been included. Adaptive voltage level at source is a technique in which the power consumption is reduced by lowering the supply potential.

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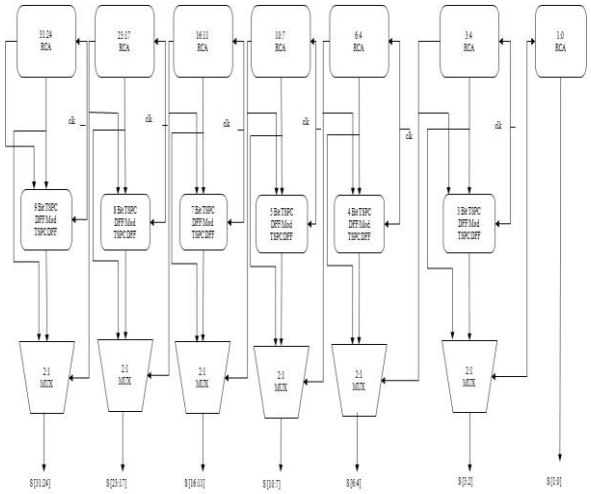

Fig.1. ***Proposed 32-bit SCSLA with AVLS-TSPC-based D flip flop***

5. Methodology

5.1 Adders

In signal processors, microprocessors, and other applications, adders play a powerful role as the fundamental arithmetic circuit. Therefore, recovering the presentation of the adders illustrate a crucial part in advancing the overall circuit.

A. *Ripple Carry Adder*

The RCA is established by dropping one-bit full adders to produce the sum as well as the carry signals. The sum and carry signals of the one-bit full adders are originated according to (1) and (2). The successive block give rise to the sum only after the previous block is summed. The carry from the prior case block is send to the subsequent blocks for addition. This construction is competent in terms of area, but the delay in production of carry signal from the prior blocks to the next, results in the adder operating at a undemanding speed. Since speed is an important factor in numerous applications, CSLA is ideal to beat the delay of RCA:

$$S = A \oplus B \oplus Carry_{in} \quad (1)$$

$$Cout = A \cdot B + B \cdot Carry_{in} + Carry_{in} \cdot A \quad (2)$$

B. Carry Select Adder with Ripple Carry Adder

The linear n-bit CSLA is alienated into m-blocks with the same bit size. But there is a incompatible delay while acquiring the carry and sum signals. In SCSLA, the n-bit adder is

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divided into m-blocks with unequal bit-size. For a 16-bit adder, it is divided into five blocks with sizes of 2, 2, 3, 4, and 5-bits in-order from the right-end block. apart from for the right-end block, all other blocks consist of two RCAs with all having carry_ in "0" and "1,"correspondingly The multiplexer (MUX) helps to rise above the unequal delay present in linear CSLA. The SCSLA performs its operation very quick as compared to RCA because it does not remain for carry from the preceding block, rather performs the addition with the autonomous given carry signal. Hence, the sum and carry outputs are obtained at the MUX output. Fig. 1 shows a 32-bit SCSLA with RCA [4].

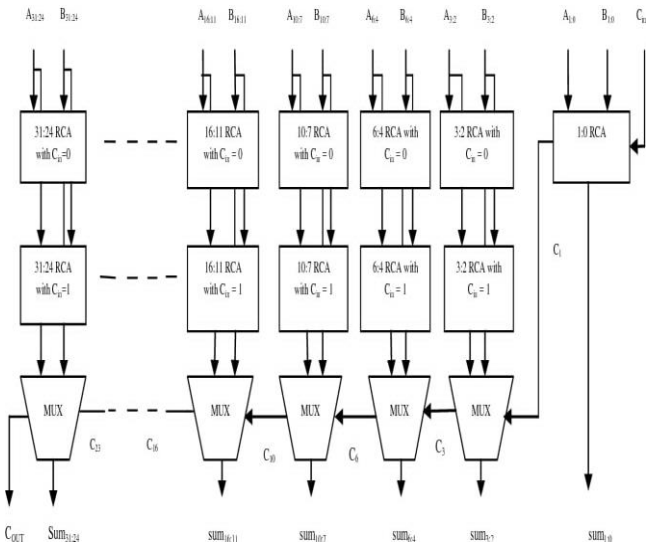

Fig. 2. 32-bit square root carry select adder (SCSLA) with ripple carry adder (RCA)

C. Square Root Carry Select Adder with TSPC-Based D-Flip Flop

The 32-bit SCSLA using the standard positive edge-triggered D-FF uses the RCA with the clock as carry_ in for addition. When the clock becomes zero, the RCA carry out the addition with carry_ in = "0," and sends the result to the D-FF. At some stage in the positive edge of the clock, this result is gathered in the D-FF. When the clock enhances high (or logic "1"), the RCA produce the addition with carry_ in = "1," and sends it straight to the multiplexer, as the D-FF acts as a latch while the clock becomes elevated. The real sum and carry are produced at the end of one entire clock cycle.

D. Adaptive Voltage Level

To attain least dissipation of power by the circuit and to make it function at low power, a method called adaptive voltage level (AVL) is used. The AVL circuit is supervised by a sleep-control signal. The AVLG uplift the potential of the ground, whereas the AVLS reduced the supply voltage potential, therefore diminishing the dissipation of power by the complete circuit. Adaptive voltage level at source consists of a parallel connection of two NMOS transistors and one PMOS transistor. The two NMOS transistors are link together in series. The clock signal is associated to the PMOS transistor node which acts as the input to

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the circuit. Inversely, the supply is fed to the input of NMOS transistors. The supplied clock performs as the sleep signal that controls the performance of the AVLS circuit.

6. Propose and Functioning of Adder Architectures

Xilinx ISE is used to execute every circuit using both 180 nm and 45 nm technologies. Modelsim is used to achieve the simulation of the structure. The SCSLA can be changed by implementing a D flip-flop as an alternative of the second RCA in each block, with a intent to reduce the consumption of power along with the delay of the SCSLA.

The D-FF can be noticed that it works rapidly by including TSPC to the D-FF. True-single phase clocking permits the true phase of the clock and does not take part of it. The SCSLA with TSPC-based D-FF is capable with reference to power, area, and delay. The standard TSPC-based D flip-flop is designed using 11. Only a single clock can be observed in TSPC which is never upturned. The clock signal is given to both NMOS and PMOS transistors. The output is regularly affected by the switching of inputs with difference in the clock. A TSPC clock reduces all the power utilization of the circuit as it needs fewer transistors, and thereby improves the speed of the circuit. True-single phase clocking performs as master and slave circuits. The SCSLA can be prepared power and speed efficient by applying D-FF rather than the RCA in the second row. The modified TSPC-based D-FF can be implemented by taking off of one transistor from the normal TSPC-based D flip-flop [5]. As the revised TSPC based D-FF can be obtained using 10 transistors, it disperse low power in difference with the normal TSPC-based D-FF.

The TSPC based D flip-flop utilizes minimum power compared to the one-bit full adder. Hence, the normal and modified TSPC-based D flip-flop is chosen over RCA in SCSLA. Considering them the goal to further reduction of power usage of the normal and changed TSPC based D flip-flop, the AVLS method can be applied. Whereas the D-FF is a sequential segment and makes use of a clock signal for its working, the same can be used as the control signal for the AVLS circuit. In the AVLS circuit, the NMOS transistors are even more in the ON state, as they are forward biased. The PMOS transistor has the clock signal as the input and hence switches from one state to the other. As a result, the least amount of discharged current flows through the PMOS of AVLS, thereby diminishing the operation of power by the circuit. Two designs have been suggested as a part of the proposed architecture. The proposed-1 design has AVLS normal TSPC-based D flip-flop and the proposed-2 design has AVLS modified TSPC-based D flip-flop these flip-flops are used as an alternative of RCA in the second row of each block in the 32-bit SCSLA. The AVLS circuit is placed in the middle of the supply voltage and the 32-bit SCSLA adder, with a clock signal as the input to the AVLS circuit.

The clock signal is similar to both AVLS and 32-bit CSLA circuits. Due to this, the outflow of the PMOS transistor is diminished, thereby reducing the dissipation of power by the entire 32-bit CSLA. When the clock is 0, the addition is executed by the RCA in the first row and the output is passed onto the D-FF. During the positive edge of the clock, the D flip-

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flop is stimulated and hence, it stores the result. When the clock becomes high, the RCA executes the addition and the result is moved directly to the multiplexer. The D-FF continues to hold the prior result, as it works as a latch when the clock is high. At the end of one complete clock cycle, the actual sum and carry are acquired at the multiplexer output with the select line as carryout of the previous block.

Results and Discussions

The AVLS normal TSPC- based d flip-flop can be implemented with 16-bit SQRT CSLA to obtain power and delay efficient adder. The amount of the power dissipated by the altered TSPC-based D-FF is reduced considerably on the implementation of AVLS logic. Fig. 7.1 shows the output waveform of the existing 16-bit SQRT CSLA with AVLS normal and modified TSPC- based D-FF. With the help of Modelsim, the addition of 16-bit is simulated and the respective outputs are taken in the form of square waveform.

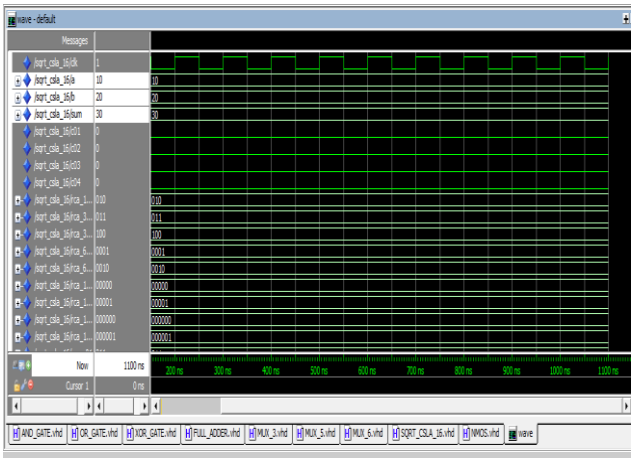

Fig 7.1 Output waveform of 16 bit SQRT CSLA

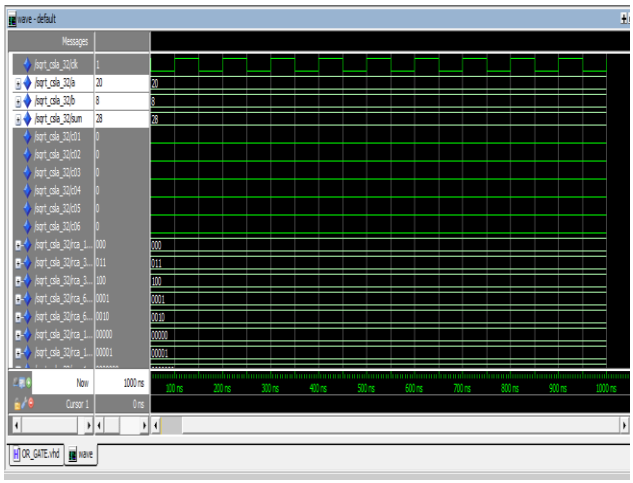

Fig 7.2 Output waveform of 32-bit SQRTCSLA

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Fig. 7.2 shows the output waveform of the proposed 32-bit SQRT CSLA with AVLS normal and modified TSPC- based D-FF. With the help of Modelsim, the addition of 32-bit SQRT CSLA is simulated and the respective outputs are taken in the form of square waveform. Set the clock as clock, and give the inputs A and B by clicking force ->10#20 and 10#8. After the simulation the output will be displayed as 28 in the form of waveforms 0's and 1's.

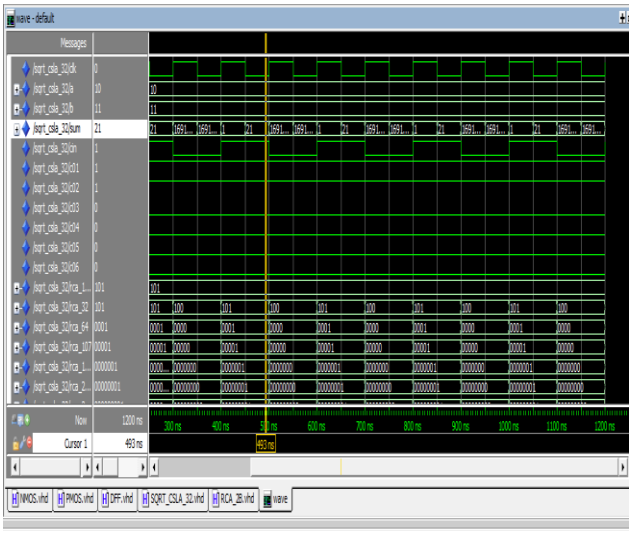

Fig.7.3 Output waveform of TSPC

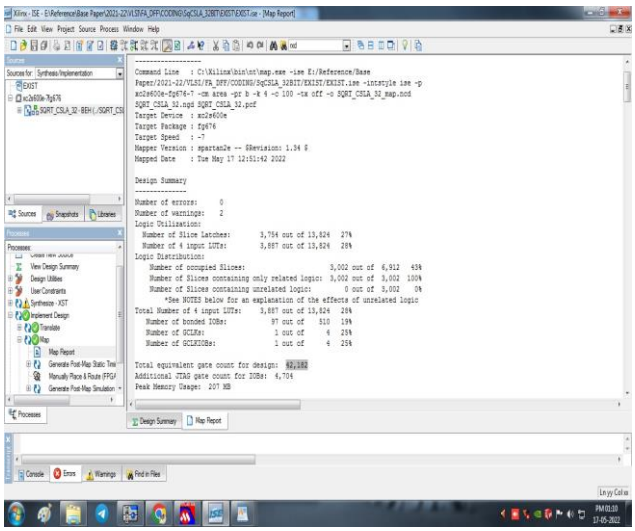

Fig. 7.4 Area calculation of the existing work

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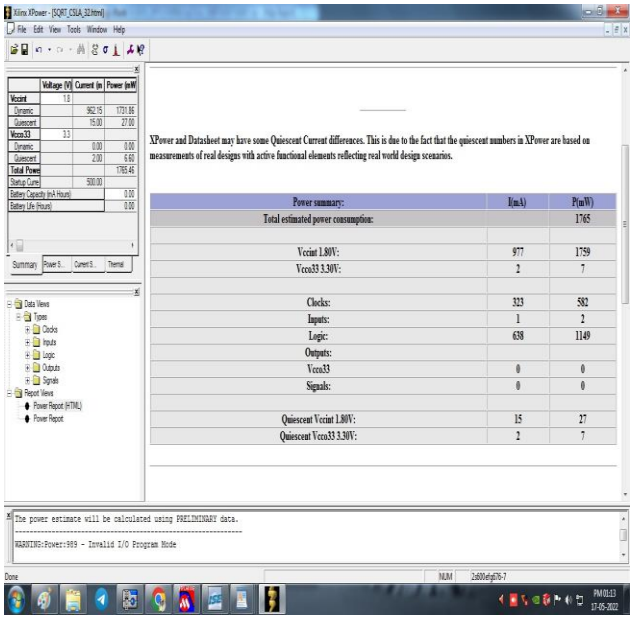

XPower and Datasheet may have some Quiescent Current differences. This is due to the fact that the quiescent numbers in XPower are based on measurements of real designs with active functional elements reflecting real world design scenarios.

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		1765
Vccint 1.80V:	977	1759
Vcco33 3.30V:	2	7
Clocks:	323	582
Inputs:	1	2
Logic:	638	1149
Outputs:		
Vcco33	0	0
Signals:	0	0
Quiescent Vccint 1.80V:	15	27
Quiescent Vcco33 3.30V:	2	7

Table.I Power output of the existing work

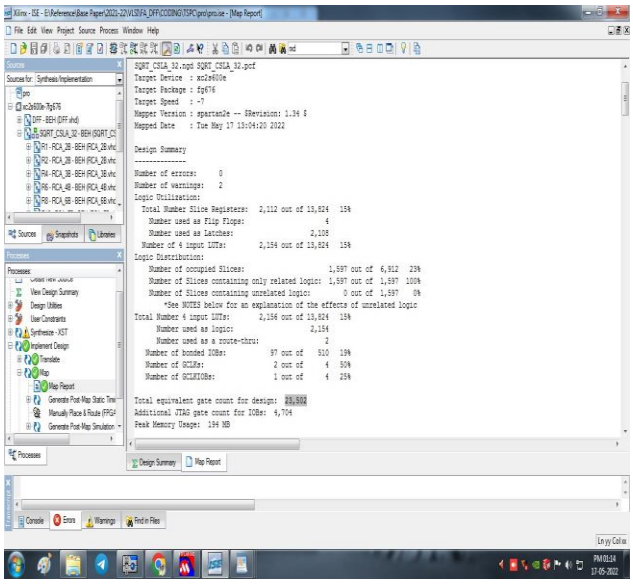

Fig.7.5 Area calculation of the proposed work

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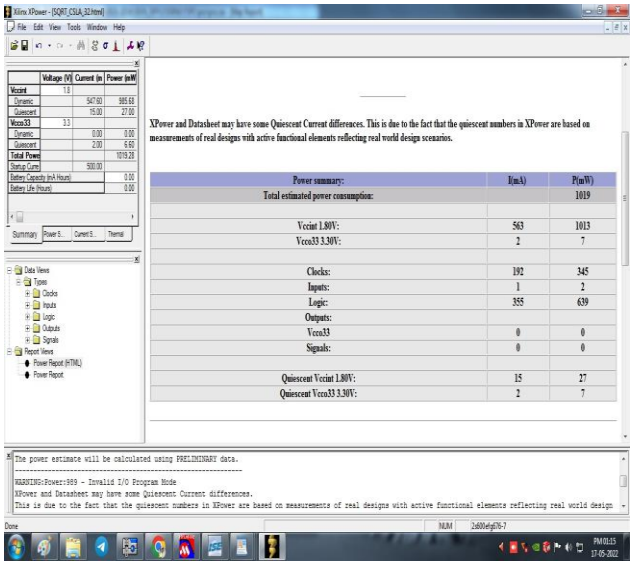

XPower and Datasheet may have some Quiescent Current differences. This is due to the fact that the quiescent numbers in XPower are based on measurements of real designs with active functional elements reflecting real world design scenarios.

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		1019
Vccint 1.80V:	563	1013
Vcco33 3.30V:	2	7
Clocks:	192	345
Inputs:	1	2
Logic:	355	639
Outputs:		
Vcco33	0	0
Signals:	0	0
Quiescent Vccint 1.80V:	15	27
Quiescent Vcco33 3.30V:	2	7

Table.II Power output of the proposed work

The adders design proposed in this paper has been developed using VHDL coding and the simulations are carried out using Modelsim. The existing and proposed architecture of the power and area are calculated using Xilinx ISE. Fig 7.4 and Fig 7.5 shows the calculation for the area of the existing and proposed design.

7. Conclusion and Scope for Future Development

The speed of the adders is related to the carry propagation mechanism. In order to weigh down the diffusion of power, and advance the rate of addition, different 32-bit adders are analyzed. All the structures are analyzed at 100 MHz in force frequency. The 32-bit SCSLA with RCA has a lesser amount of delay but consumes extra power as compared to 32-bit RCA. To reduce the power utilization, the RCA in SCSLA is replaced with a D flip-flop, which yields a smaller amount power as well as less delay. Modified TSPC-based D flip-flop is used to get relatively less delay and power than 32-bit SCSLA with normal TSPC-based D flip-flop. It can be concluded that the 32-bit SCSLA with AVLS normal and modified TSPC-based D flip-flop consumes the less amount of power among all other adders when applied in 45 nm technology. The adders can be further extended as upcoming work, for 64-bit, and 128-bit, and can be implemented in partitioned Dadda multipliers and other complex architectures, which play a vital role in DSP applications.

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